Remarks

The various parts of the Office Action (and other matters, if any) are discussed below under appropriate headings.

Claim Rejections - 35 USC § 101

Claims 1-2 stand rejected under 35 USC §101 as being directed to non-statutory subject matter. In particular, the Examiner states that the claims are directed to a computer program *per se*.

By way of the foregoing amendments, claims 1 and 2 have been amended to remove any issue as to the alleged non-statutory subject matter and therefore the rejection is moot.

Accordingly, withdrawal of the rejection of claims 1 and 2 is respectfully requested.

Claim Rejections - 35 USC § 103

Claims 1, 3 and 6-9 stand rejected under 35 USC §103(a) based on U.S. Patent No. 5,982,887 (*Hirotani*) in view of U.S. Patent No. 6,907,125 (*Oishi*) in further view of Applied Cryptography (*Schneier*), and in further view of U.S. Patent No.6,526,462 (*Elabd*). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 1 has been amended to clarify that the data scramble circuit is a single hardware circuit and at least a portion of the data scramble circuit is operative to perform both a data scramble function and an error correction function. For example, the data scramble circuit can be an error correction circuit that is used to perform error correction functions. Further, that same error correction circuit can be used to perform data scramble functions (see pg. 8, lns. 7-10 of the specification). Thus, a single circuit can be used to performed two different functions.

Elabd teaches that circuits can be implemented using a "system on chip" (SOC) design, as opposed to traditional, separate component integrated circuit designs. In other words, multiple functions that may have been implemented on separate chips are implemented on a single chip. The SOC design of *Elabd*, however, still retains the

individual circuits that perform specific operations (e.g., an I/O control circuit performs I/O control operations, a memory control circuit performs memory control operations, etc., see Fig. 2 of *Elabd*). Each of these individual circuits performs a single dedicated function. *Elabd* does not teach or suggest a data scramble circuit comprises a single hardware circuit and at least a portion of the data scramble circuit is operative to perform both a data scramble function and an error correction function, as recited in amended claim 1.

The remaining art to *Hirotani*, *Oishi* and *Schneier* does not make up for the above deficiencies of *Elabd*. Similar comments apply to independent claims 3, 6 and 8.

Accordingly, withdrawal of the rejection of claims 1, 3, 6 and 8 is respectfully requested.

Claims 2, 5, 7 and 9 depend from one of the above claims and, therefore, can be distinguished from the cited art for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 2, 5, 7 and 9 is respectfully requested.

Conclusion

In view of the foregoing, request is made for timely issuance of a notice of allowance.

Respectfully submitted,

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